ISSUE NO. 5 • SEPTEMBER-OCTOBER 1992

Futurebus+ Design

HYBRICON SOLVES THE 2.1-VOLT NOISE PROBLEM

The following is a reprint of the article "Futurebus+ Trouble Report: Noise at 2.1V" published in *Futurebus+ Design*, No. 5, September/October 1992.

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At a recent IEEE Futurebus+ meeting in California, a paper was circulated describing serious inter-module communication problems which had been observed in FB+ systems containing multiple CPU and memory cards.

The problems have been attributed to excessive voltage transients found on the termination power supply. These result primarily from the inability of the power supply to regulate its output in response to large switching transients, such as those encountered when 64 or more signal lines change state at the same time.

To help explain how the dynamic behavior of the termination power supply affects system performance, we will first present some theory.

Figure 1 shows a simplified representation of the backplane signal termination system. The termination power supply is represented by an ideal voltage source, V_t, and a series impedance, Z_s. The impedance Z_s represents the sum of the power-supply impedance and the impedance of the bypass and stray capacitance and path inductances on the backplane. The termination resistors for the open-collector signal lines are represented as $R_{t1}...R_{tn}$. V_s is the AC component of the voltage on the supply side of each terminating resistor.

Consider the case where all of the signal lines are high, that is, none of the BTL drivers on the bus are pulling any of the lines low. In this condition,

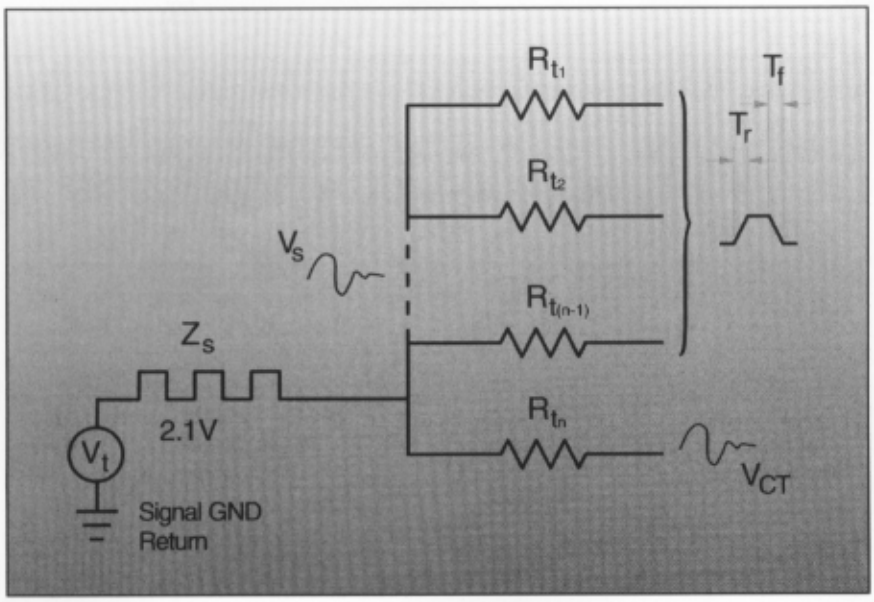

Figure 1. *Model of the signal termination system for a Futurebus+ backplane.*

the voltage source supplies essentially no current and V_s=0.

Now suppose the signal lines associated with R_{t1}, R_{t2}, ...$R_{t(n-1)}$ all are driven low simultaneously (worst case). A voltage will appear across Z_s that will reduce the voltage V_s seen by the signal line associated with R_n:

$$V_s = Z_s(T_r,T_f)\sum_{j=1}^{n-1} I_j(T_r,T_f).$$

Z_s has been written to show explicitly its dependence on the rise and fall times of the signal transitions. As the speed of the signal edges increases (T_r and T_f get smaller), the magnitude of V_s will increase.

From the above equation, we see that the fluctuations on the termination voltage, V_s, depend on Z_s and the number of switching signal lines. But, in practical supplies, the source voltage, V_t, will also fluctuate if the load current changes too rapidly. Therefore, the ability of the power supply to regulate its output under rapidly varying load conditions will also impact termination voltage.

For transients of shorter duration than the bus propagation time, the crosstalk voltage seen on signal line 1 by a module on the bus will be

$$V_{ct} = V_s \frac{Z_0''}{Z_0'' + R_n}.$$

Here, Z_0'' is the impedance of the loaded bus. For longer transients,

$$V_{ct} = V_s.$$

This assumes V_s is the same at both termination supplies.

It can be seen from the equations above that transitions on some lines will change the levels on all other lines to some degree. These changes represent noise whose magnitude depends on Z_s and the inability of the power supply to accommodate rapid changes in current demand (large *di/dt*). The *di/dt* requirement of the backplane increases with edge speed, frequency, and number of simultaneous signal transitions. If the noise is large enough, false logic levels will result, which in turn can cause system failure.

As a practical matter, the behavior of the backplane termination voltage is a function of the backplane design, value and type of the bypass capacitors, the power supply design, and the interconnection path between the power supply and the backplane. In switching power supplies where the speed of the regulator feedback loop is generally limited by a relatively slow oscillator, very fast changes in current demand will cause significant voltage fluctuations. And, when a very large change in net current demand on the supply occurs, the seemingly small reactive components of Z_s cause significant voltage drops that increase the amount of noise even further.

IMPACT ON PRACTICAL SYSTEMS

In slower backplane architectures such as VME and MBII, generous transmission settling time requirements allow the termination power system up to 30 nanoseconds to respond to the rapidly changing current demand caused by signal transitions. Under some conditions, however, simultaneous line switching can cause a change in current demand (*di/dt*) in excess of 52 Amps/μsec. This is beyond the capability of most power supplies, so conventional systems exploit the intrinsic capacitance between the ground and power planes and employ capacitors in the termination circuits to minimize power supply noise and ensure reliability.

Compare this to the situation on a Futurebus+ backplane, where incident-wave switching is required. In order to switch within 2 nanoseconds as required, the BTL signal lines as a group will impose a *di/dt* requirement on the power supply of about 6,300 Amps/μsec! (This is the case when all 128 data and 71 control signal lines in a Profile A system are asserted at once.)

The noise problem is most severe when all of the signal levels are changing together from either low to high or high to low. When the BTL transceivers are switched low, for example, the power supply must sense the almost instantaneous change in load and regulate quickly enough to avoid undershoot. Unfortunately, a typical commercial 50–100 kHz switcher has a response time in the order of

100–200 μsec rather than the 2 to 4 nanoseconds required by a Futurebus+ system.

RESULTS

How bad is it really? Back when we first suspected the problem, we at Hybricon undertook a simulation effort to investigate the potential magnitude of the noise. Figure 2a shows a result of a simulation based on a conventional power supply driving a backplane that incorporates the recommendations of IEEE 896.2. The waveforms show the power supply noise caused by simultaneous switching of 128 lines. Here, the lines each pass a 500nsec-wide pulse once every 4 microseconds. For this case, the noise voltage (greater than 400 mV peak-to-peak) could clearly cause problems.

Figure 2b is an oscilloscope photograph showing power supply noise in an actual system. Here, two processor modules accessed a shared memory module using a 64-bit data bus. The measurement was made at the termination end of the bus line. The simulation and the actual waveforms are quite similar.

The extreme terminator power requirements for Futurebus+ demand a system design approach which considers the backplane, power routing, and power supply as three elements of a tightly coupled system. Each must be carefully designed and integrated with the others to guarantee adequate noise margin.

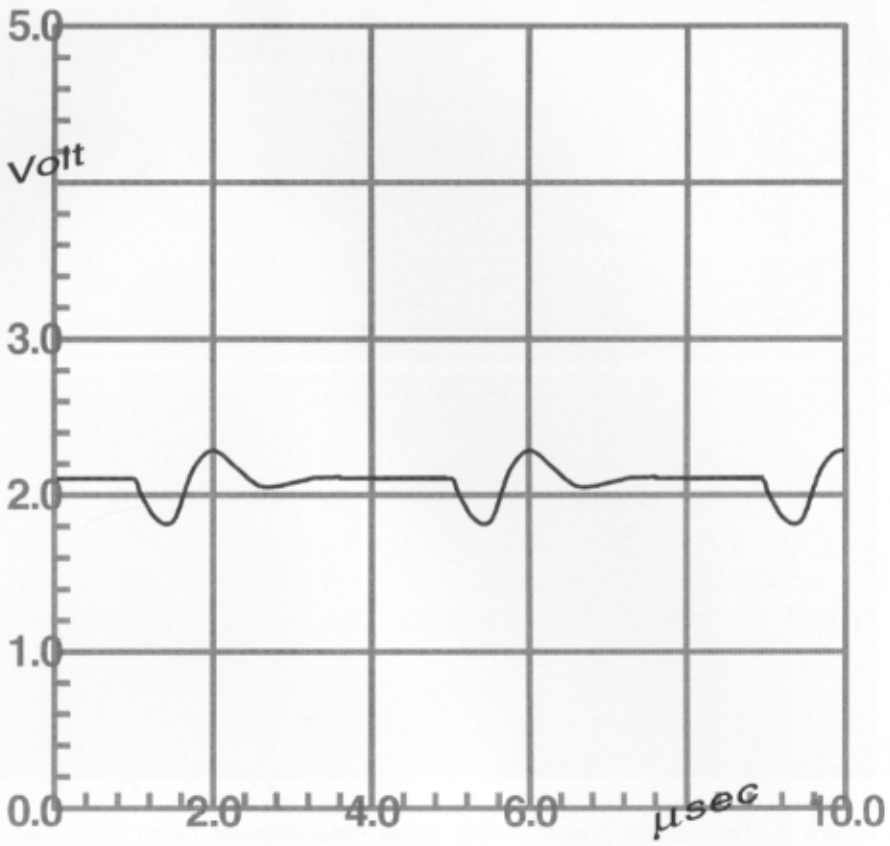

Figure 2a. *Result of a simulation based on a conventional power supply driving a Futurebus+ backplane. The waveform shows the power supply noise caused by simultaneous switching of 128 lines.*

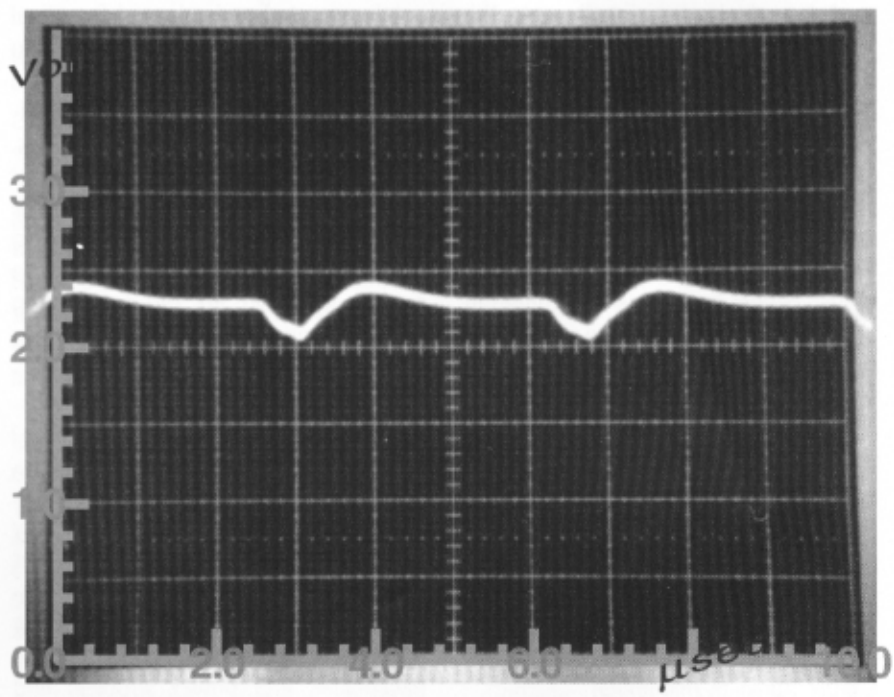

Figure 2b. *Oscilloscope photograph showing power supply noise in an actual system, with two processor modules accessing shared memory through a 64-bit data bus. The noise level is similar to that predicted by the simulation.*

A SOLUTION FOR FUTUREBUS+ SYSTEMS

At Hybricon, we've anticipated the power supply problem since first raising the issue in 1990 at a Futurebus+ meeting. Accordingly, we have developed a power supply and backplane system that will regulate the signal terminator voltage to within ±24 mV of specification.

The Hybricon system consists of a high-quality FB+ backplane and two

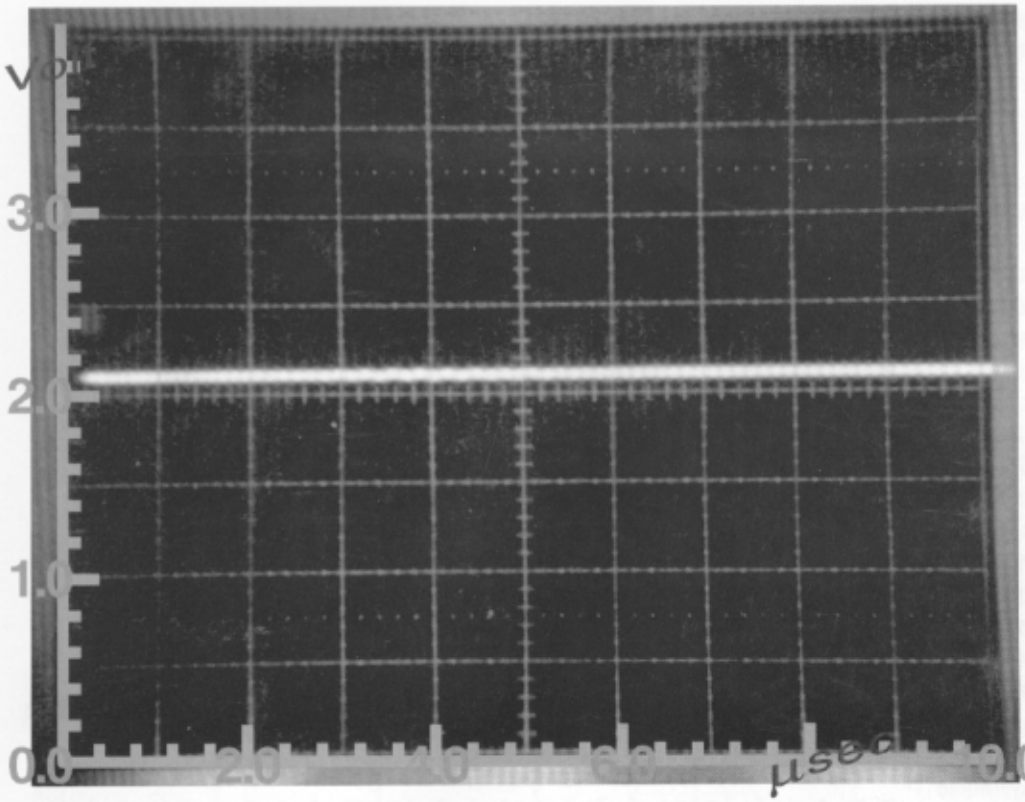

Figure 3. *Termination power supply noise measurement taken while two processor modules access shared memory in a system with Hybricon's improved backplane/power supply. As shown, power supply noise is negligible.*

uniquely designed 2.1V power supply modules which plug directly onto the rear of the backplane at each end, in the area of the termination circuitry. These "super response" power supplies can respond to changes in current demand well in excess of 200 Amps/μsec. This, combined with large amounts of distributed capacitance in the termination system, results in a power-supply/backplane combination that has been shown to be capable of meeting all anticipated demands.

The system has been tested at the Johns Hopkins University Applied Physics Laboratory (JHU/APL) under actual system conditions, with two processor boards and a shared memory board communicating over a 64-bit bus. The waveform photograph in Figure 3 shows data taken during tests at JHU/APL. As shown, power supply noise is negligible.

Additional testing has been carried out to estimate performance in a 128-bit system. In one case, all 128 data lines and 71 control lines were alternately asserted and released for equal periods at a frequency from 1 kHz to 20 MHz. Under these conditions, the Hybricon system demonstrated a maximum noise voltage of 24 mV peak. The results were presented at the last Futurebus+ meeting to demonstrate that the Hybricon backplane is able to perform well within the ±50 mV noise margin specified for the termination power supply, even under worst-case conditions.

CONCLUSION

The high-performance afforded by Futurebus+ systems has placed great demands on backplane and power-supply design. In the past, designers have been able to independently optimize backplanes and power supplies and then integrate them into systems. Now with the more stringent demands of incident wave switching, it has become necessary to design the backplane and power supply together. Further, finite analysis and SPICE modeling may be required to effectively carry out these designs.

The Futurebus+ standard (IEEE 896.2) makes some general statements regarding the importance of characterizing the dynamic behavior of the termination power supply, and it even suggests that system manufacturers specify the capabilities of their systems. However, specific test requirements are not given. For this reason, a study group was formed to make specific recommendations in order that FB+ systems shall be tested to ensure that the designs are adequate. Hopefully, this group will define standard measurement methods and *di/dt* requirements for 32-bit, 64-bit, and 128-bit systems that will guarantee conformance with the 50 mV peak-to-peak noise specification. ■

C. Michael Hayward is the President, David Dai is senior scientist, and Michael Munroe is marketing specialist at Hybricon Corporation. *The authors wish to acknowledge the generous assistance of Ed Jacques and Richard Lopez of the Johns Hopkins University Applied Physics Laboratory and Erasmo Brenes of Cable & Computer Technology, Inc.*